LME49710 High Performance, High Fidelity Audio Operational Amplifier

Check for Samples: LME49710

FEATURES

- **Easily drives 600Ω loads**
- **Optimized for superior audio signal fidelity**
- **Output short circuit protection**
- **PSRR and CMRR exceed 120dB (typ)**
- **SOIC, DIP, TO-99 metal can packages**

APPLICATIONS

- **Ultra high quality audio amplification**
- **High fidelity preamplifiers**
- **High fidelity multimedia**
- **State of the art phono pre amps**
- **High performance professional audio**
- **High fidelity equalization and crossover networks**
- **High performance line drivers**
- **High performance line receivers**
- **High fidelity active filters**

DESCRIPTION

The LME49710 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state-of-the-art circuit design, the LME49710 audio operational amplifiers deliver superior audio signal amplification for outstanding audio performance. The LME49710 combines extremely low voltage noise density (2.5nV/$\sqrt{Hz}$) with vanishingly low THD+N (0.00003%) to easily satisfy the most demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49710 has a high slew rate of ±20V/μs and an output current capability of ±26mA. Further, dynamic range is maximized by an output stage that drives 2kΩ loads to within 1V of either power supply voltage and to within 1.4V when driving 600Ω loads.

The LME49710's outstanding CMRR(120dB), PSRR(120dB), and V_{OS} (0.05mV) give the amplifier excellent operational amplifier DC performance.

The LME49710 has a wide supply range of ±2.5V to ±17V. Over this supply range the LME49710's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49710 is unity gain stable. The Audio Operational Amplifier achieves outstanding AC performance while driving complex loads with values as high as 100pF.

The LME49710 is available in 8–lead narrow body SOIC, 8–lead plastic DIP, and 8–lead metal can TO-99. Demonstration boards are available for each package.

Table 1. Key Specifications

	VALUE	UNIT
■ Power Supply Voltage Range	±2.5 to ±17	V
■ THD+N (A_V = 1, V_{OUT} = 3V_{RMS}, f_{IN} = 1kHz)		
R_L = 2kΩ	0.00003% (typ)	
R_L = 600Ω	0.00003% (typ)	
■ Input Noise Density	2.5	nV/√Hz (typ)
■ Slew Rate	±20)	V/μs (typ
■ Gain Bandwidth Product	55	MHz (typ)
■ Open Loop Gain (R_L = 600Ω)	140	dB (typ)
■ Input Bias Current	7	nA (typ)
■ Input Offset Voltage	0.05	mV (typ)

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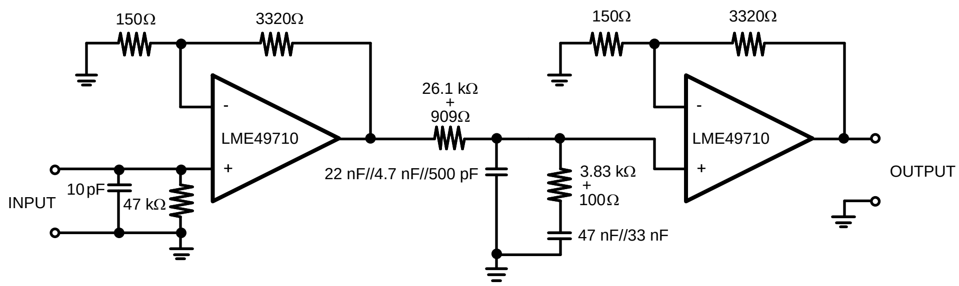
Table 1. Key Specifications (continued)

■ DC Gain Linearity Error	0.000009%	

Typical Application



Note: 1% metal film resistors, 5% polypropylene capacitors

Figure 1. Passively Equalized RIAA Phono Preamplifier

Connection Diagram

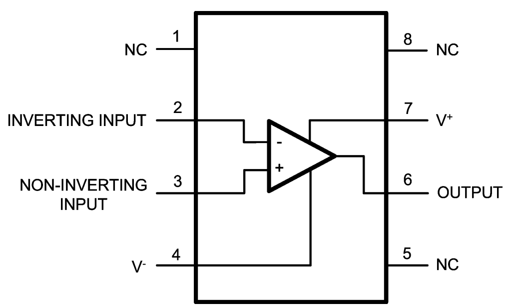


Figure 2. Diagram

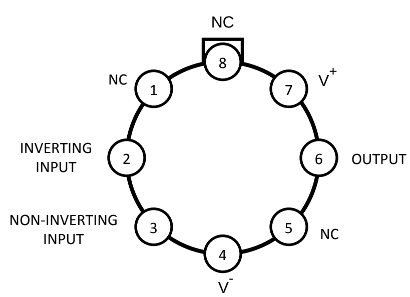


Figure 3. Metal Can

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1) (2)

Power Supply Voltage ($V_S = V^+ - V^-$)	36V
Storage Temperature	−65°C to 150°C
Input Voltage	(V-) - 0.7V to (V+) + 0.7V
Output Short Circuit(3)	Continuous
Power Dissipation	Internally Limited
ESD Susceptibility(4)	2000V
ESD Susceptibility(5)	200V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (SO)	145°C/W
θ_{JA} (NA)	102°C/W
θ_{JA} (HA)	150°C/W
θ_{JC} (HA)	35°C/W
Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage Range	$\pm 2.5V \le V_S \le \pm 17V$

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) Amplifier output connected to GND, any number of amplifiers within a package.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage and then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

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Electrical Characteristics

(1)(2)

The following specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LME49710 Typical (3)	LME49710 Limit (4) (5)	Units (Limits)
THD+N	Total Harmonic Distortion + Noise	A_V = 1, V_{OUT} = $3V_{RMS}$ R_L = 2kΩ R_L = 600Ω	 0.00003 0.00003	 0.00009	 % (max) % (max)
IMD	Intermodulation Distortion	A_V = 1, V_{OUT} = $3V_{RMS}$ Two-tone, 60Hz & 7kHz 4:1	0.00005		% (max)
GBWP	Gain Bandwidth Product		55	45	MHz (min)
SR	Slew Rate		±20	±15	V/μs (min)
FPBW	Full Power Bandwidth	V_{OUT} = $1V_{P-P}$, –3dB referenced to output magnitude at f = 1kHz	10		MHz
t_s	Settling time	A_V = 1, 10V step, C_L = 100pF 0.1% error range	1.2		μs
e_n	Equivalent Input Noise Voltage	f_{BW} = 20Hz to 20kHz	0.34	0.65	μV_{RMS}
	Equivalent Input Noise Density	f = 1kHz f = 10Hz	2.5 6.4	4.7	nV/√Hz nV/√Hz
i_n	Current Noise Density	f = 1kHz f = 10Hz	1.6 3.1		pA/√Hz pA/√Hz
V_{OS}	Offset Voltage		±0.05	±0.7	mV (max)
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	40°C ≤ T_A ≤ 85°C	0.2		μV/°C
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage	ΔV_S = 20V (6)	125	110	dB (min)
I_B	Input Bias Current	V_{CM} = 0V	7	72	nA (max)
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	–40°C ≤ T_A ≤ 85°C	0.1		nA/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	5	65	nA (max)
V_{IN-CM}	Common-Mode Input Voltage Range		+14.1 –13.9	(V+) – 2.0 (V-) + 2.0	V (min) V (min)
CMRR	Common-Mode Rejection	–10V<V_{CM}<10V	120	110	dB (min)
Z_{IN}	Differential Input Impedance		30		kΩ
	Common Mode Input Impedance	–10V<V_{CM}<10V	1000		MΩ
A_{VOL}	Open Loop Voltage Gain	–10V<V_{OUT}<10V, R_L = 600Ω	140		dB
		–10V<V_{OUT}<10V, R_L = 2kΩ	140	125	dB
		–10V<V_{OUT}<10V, R_L = 10kΩ	140		dB
V_{OUTMAX}	Maximum Output Voltage Swing	R_L = 600Ω	±13.6	±12.5	V
		R_L = 2kΩ	±14.0		V
		R_L = 10kΩ	±14.1		V
I_{OUT}	Output Current	R_L = 600Ω, V_S = ±17V	±26	±23	mA (min)
I_{OUT-CC}	Short Circuit Current		+53 –42		mA mA

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) Typical specifications are specified at +25ºC and represent the most likely parametric norm.
(4) Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.
(6) PSRR is measured as follows: V_{OS} is measured at two supply voltages, ±5V and ±15V. PSRR = $|20\log(\Delta V_{OS}/\Delta V_S)|$.

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Electrical Characteristics (continued)

(1) (2)

The following specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LME49710		Units (Limits)
			Typical (3)	Limit (4) (5)	
R_{OUT}	Output Impedance	f_{IN} = 10kHz Closed-Loop Open-Loop	 0.01 13		 Ω Ω
C_{LOAD}	Capacitive Load Drive Overshoot	100pF	16		%
I_S	Quiescent Current	I_{OUT} = 0mA	4.8	5.5	mA (max)

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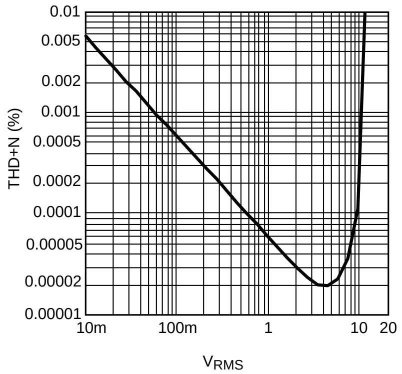
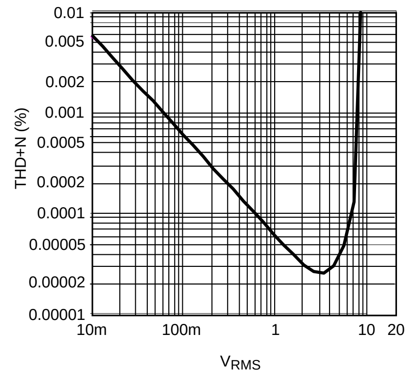
Typical Performance Characteristics

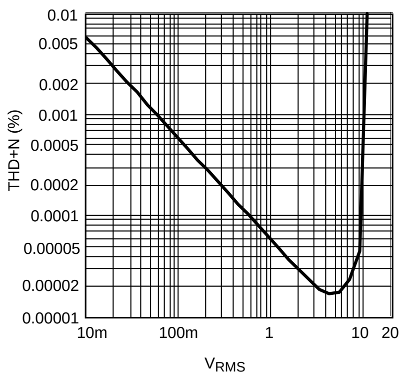
THD+N vs Output Voltage V_{CC} = 15V, V_{EE} = –15V, R_L = 2kΩ



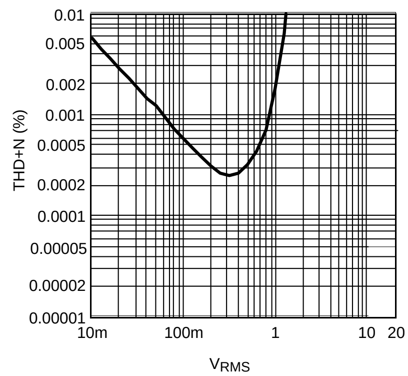
THD+N vs Output Voltage V_{CC} = 12V, V_{EE} = –12V, R_L = 2kΩ



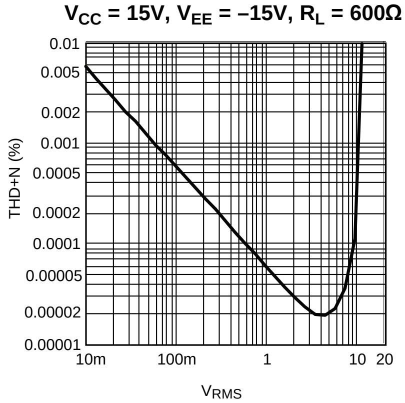
THD+N vs Output Voltage V_{CC} = 17V, V_{EE} = –17V, R_L = 2kΩ



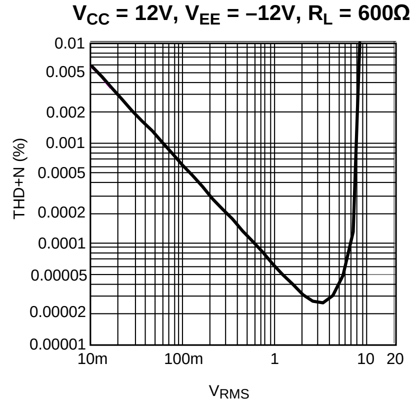
THD+N vs Output Voltage V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 2kΩ



THD+N vs Output Voltage V_{CC} = 15V, V_{EE} = –15V, R_L = 600Ω



THD+N vs Output Voltage V_{CC} = 12V, V_{EE} = –12V, R_L = 600Ω



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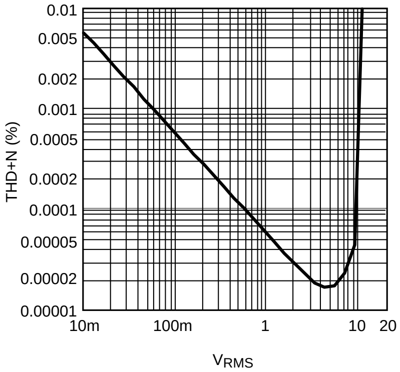
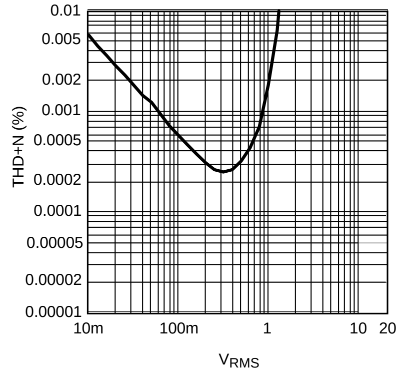
Typical Performance Characteristics (continued)

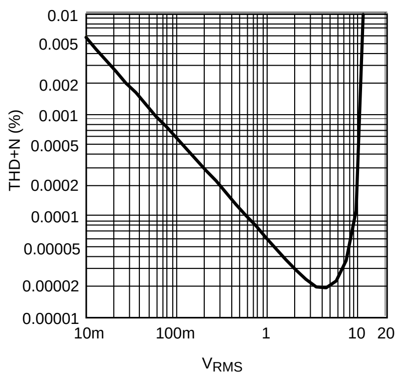
THD+N vs Output Voltage
V_{CC} = 17V, V_{EE} = –17V, R_L = 600Ω



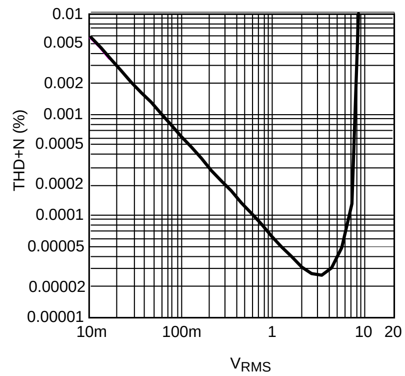
THD+N vs Output Voltage
V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 600Ω



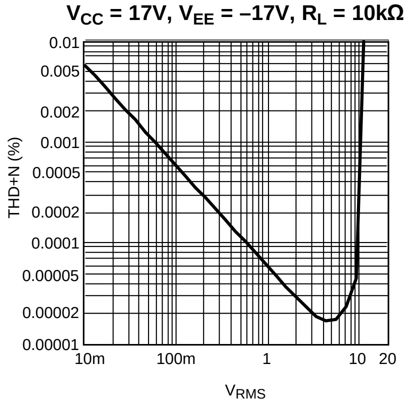
THD+N vs Output Voltage
V_{CC} = 15V, V_{EE} = –15V, R_L = 10kΩ



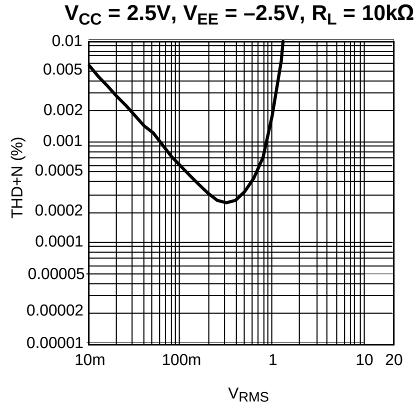
THD+N vs Output Voltage
V_{CC} = 12V, V_{EE} = –12V, R_L = 10kΩ



THD+N vs Output Voltage
V_{CC} = 17V, V_{EE} = –17V, R_L = 10kΩ

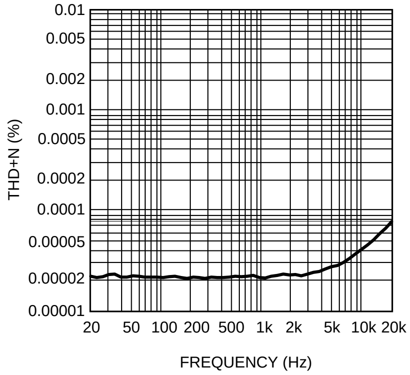


THD+N vs Output Voltage
V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 10kΩ

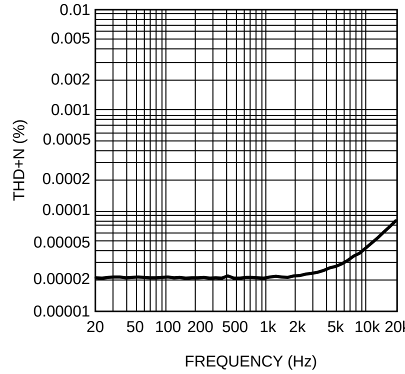


Typical Performance Characteristics (continued)

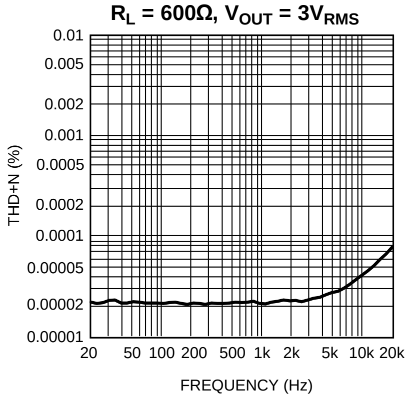
THD+N vs Frequency
V_{CC} = 15V, V_{EE} = –15V, R_L = 2kΩ, V_{OUT} = 3V_{RMS}



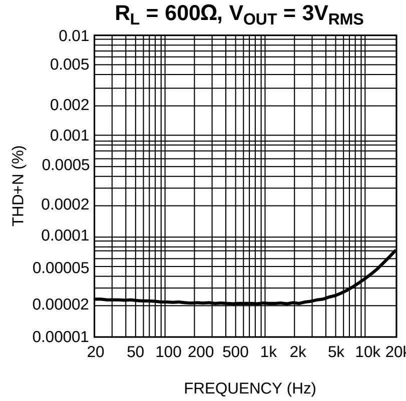
THD+N vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 2kΩ, V_{OUT} = 3V_{RMS}



THD+N vs Frequency
V_{CC} = 15V, V_{EE} = –15V, R_L = 600Ω, V_{OUT} = 3V_{RMS}



THD+N vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 600Ω, V_{OUT} = 3V_{RMS}



THD+N vs Frequency
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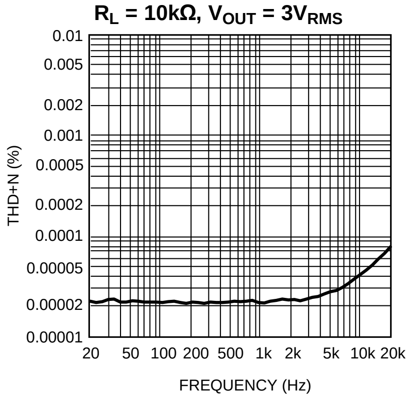
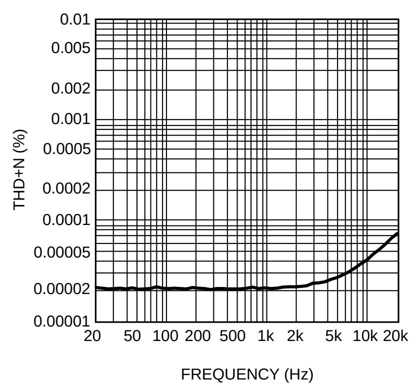


THD+N vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 10kΩ, V_{OUT} = 3V_{RMS}



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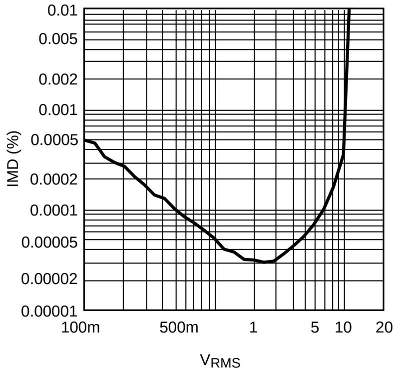
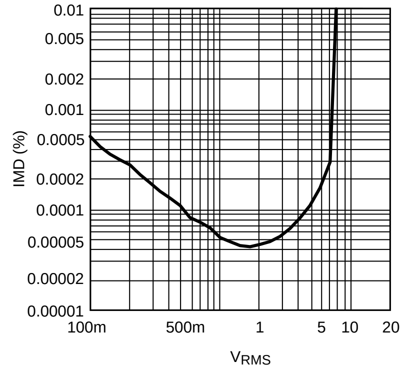
Typical Performance Characteristics (continued)

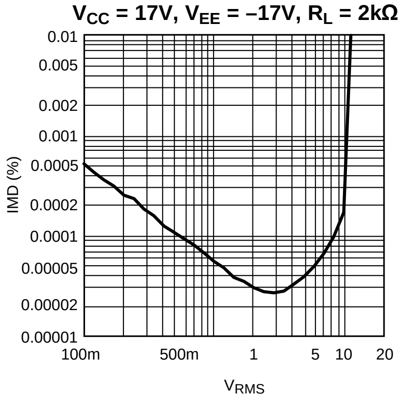
IMD vs Output Voltage V_{CC} = 15V, V_{EE} = –15V, R_L = 2kΩ



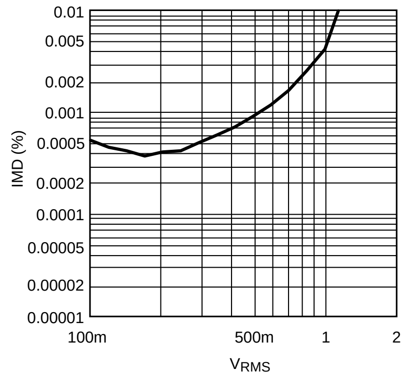
IMD vs Output Voltage V_{CC} = 12V, V_{EE} = –12V, R_L = 2kΩ



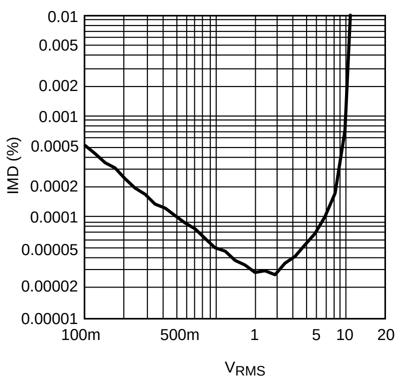
IMD vs Output Voltage V_{CC} = 17V, V_{EE} = –17V, R_L = 2kΩ



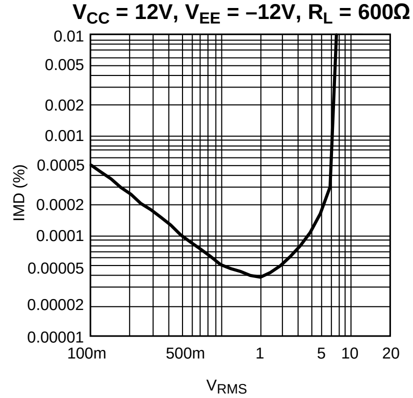
IMD vs Output Voltage V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 2kΩ



IMD vs Output Voltage V_{CC} = 15V, V_{EE} = –15V, R_L = 600Ω

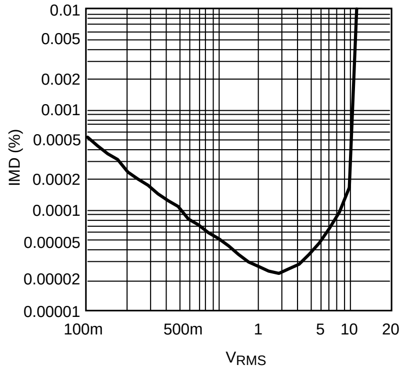


IMD vs Output Voltage V_{CC} = 12V, V_{EE} = –12V, R_L = 600Ω

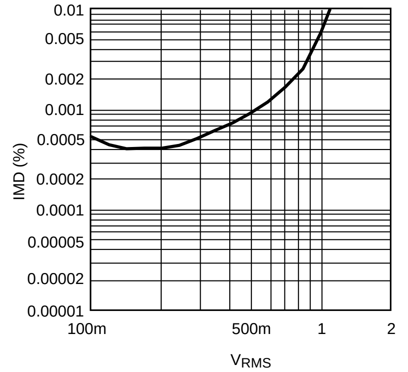


Typical Performance Characteristics (continued)

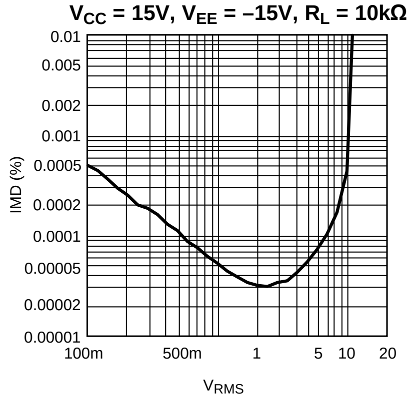
IMD vs Output Voltage
V_{CC} = 17V, V_{EE} = –17V, R_L = 600Ω



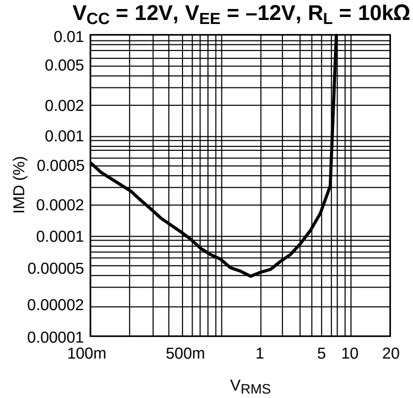
IMD vs Output Voltage
V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 600Ω



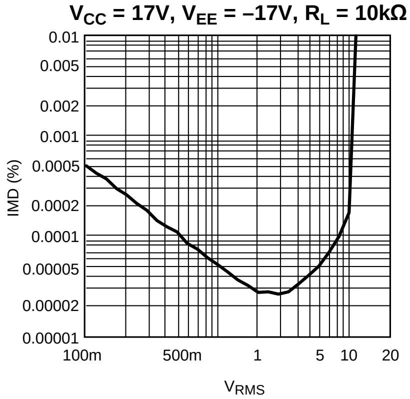
IMD vs Output Voltage
V_{CC} = 15V, V_{EE} = –15V, R_L = 10kΩ



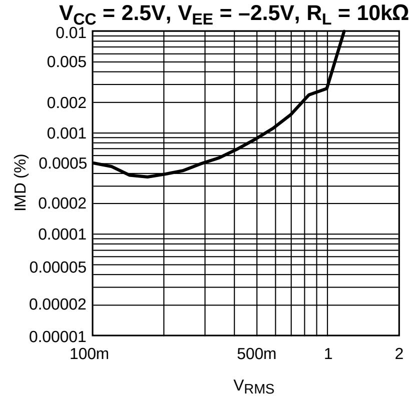
IMD vs Output Voltage
V_{CC} = 12V, V_{EE} = –12V, R_L = 10kΩ



IMD vs Output Voltage
V_{CC} = 17V, V_{EE} = –17V, R_L = 10kΩ



IMD vs Output Voltage
V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 10kΩ



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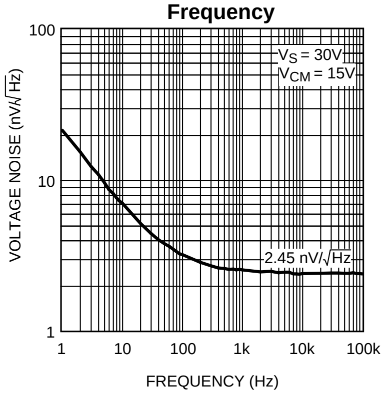
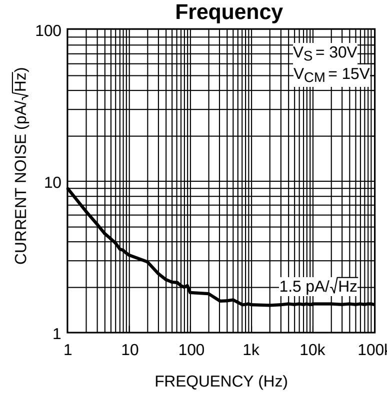
Typical Performance Characteristics (continued)

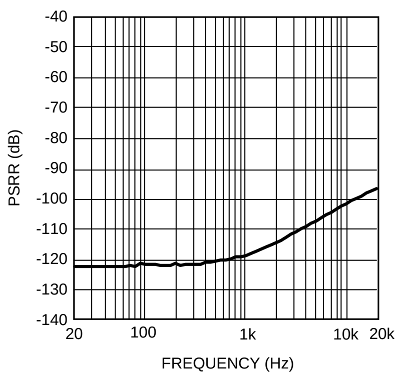
Voltage Noise Density vs Frequency



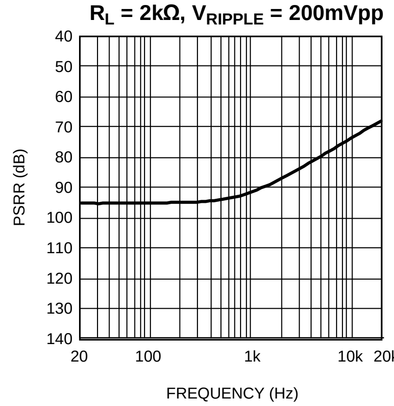
Current Noise Density vs Frequency



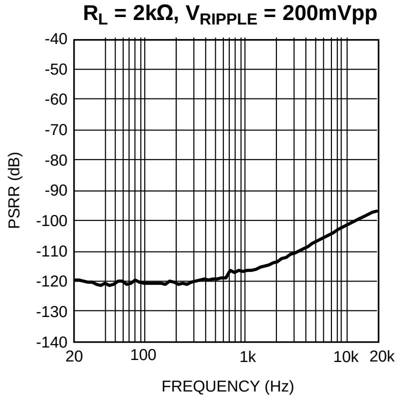
PSRR+ vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 2kΩ, V_{RIPPLE} = 200mVpp



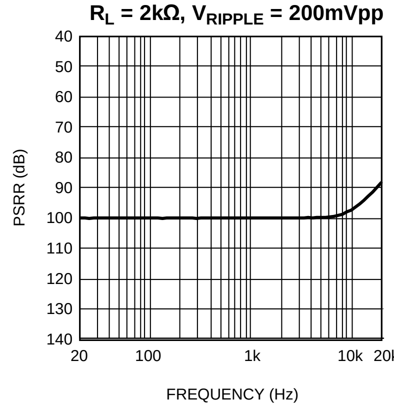
PSRR- vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 2kΩ, V_{RIPPLE} = 200mVpp



PSRR+ vs Frequency V_{CC} = 12V, V_{EE} = –12V, R_L = 2kΩ, V_{RIPPLE} = 200mVpp

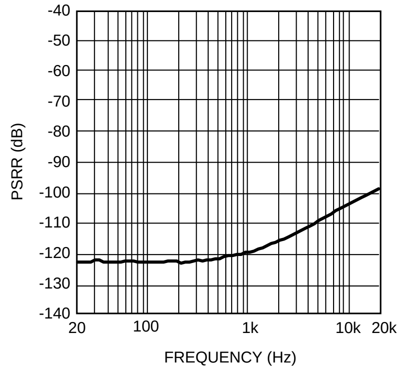


PSRR- vs Frequency V_{CC} = 12V, V_{EE} = –12V, R_L = 2kΩ, V_{RIPPLE} = 200mVpp

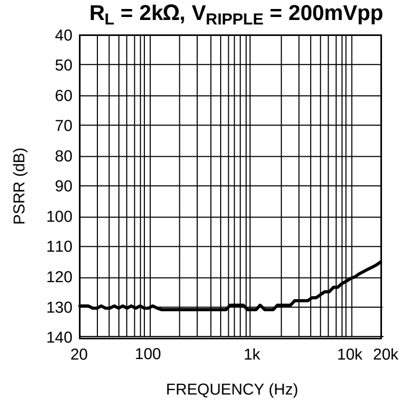


Typical Performance Characteristics (continued)

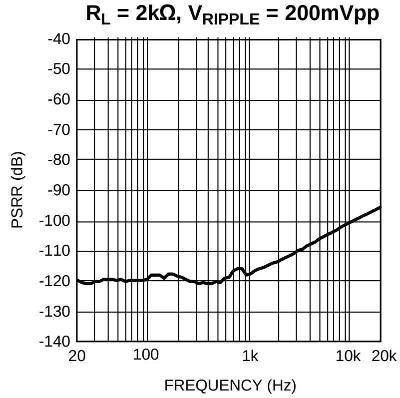
PSRR+ vs Frequency
V_{CC} = 15V, V_{EE} = –15V, R_L = 2kΩ, V_{RIPPLE} = 200mVpp



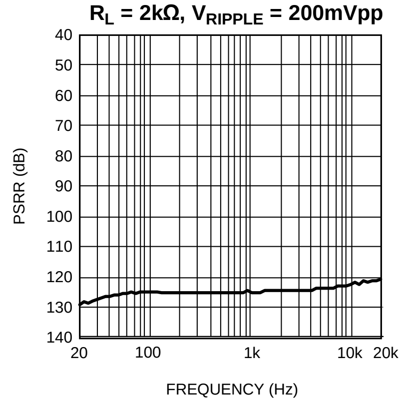
PSRR- vs Frequency
V_{CC} = 15V, V_{EE} = –15V, R_L = 2kΩ, V_{RIPPLE} = 200mVpp



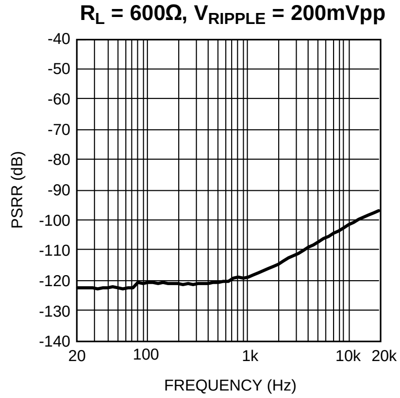
PSRR+ vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 2kΩ, V_{RIPPLE} = 200mVpp



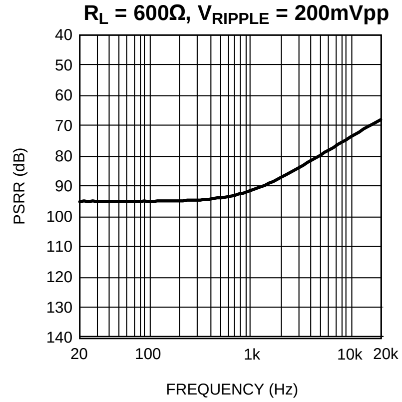
PSRR- vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 2kΩ, V_{RIPPLE} = 200mVpp



PSRR+ vs Frequency
V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 600Ω, V_{RIPPLE} = 200mVpp



PSRR- vs Frequency
V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 600Ω, V_{RIPPLE} = 200mVpp



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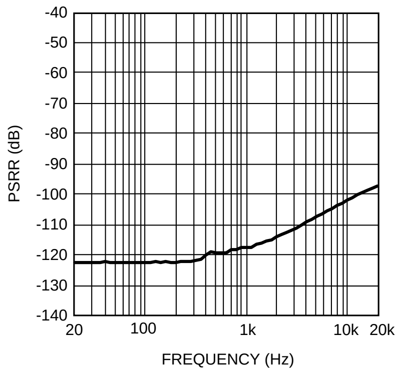
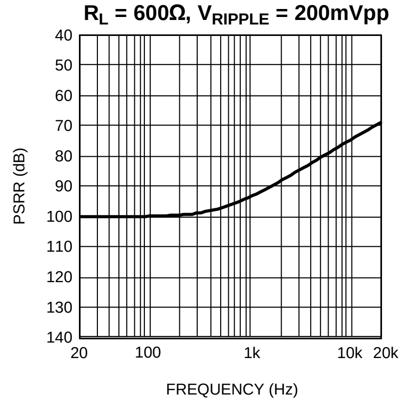
Typical Performance Characteristics (continued)

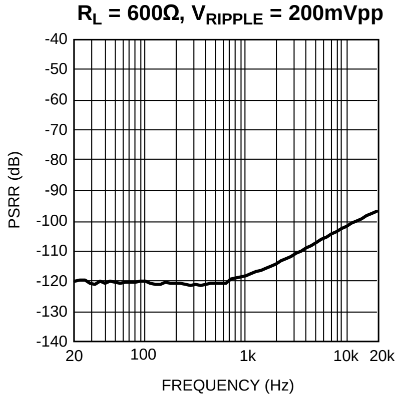
PSRR+ vs Frequency
V_{CC} = 12V, V_{EE} = –12V, R_L = 600Ω, V_{RIPPLE} = 200mVpp



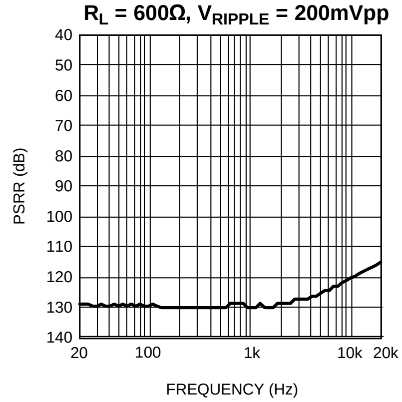
PSRR- vs Frequency
V_{CC} = 12V, V_{EE} = –12V, R_L = 600Ω, V_{RIPPLE} = 200mVpp



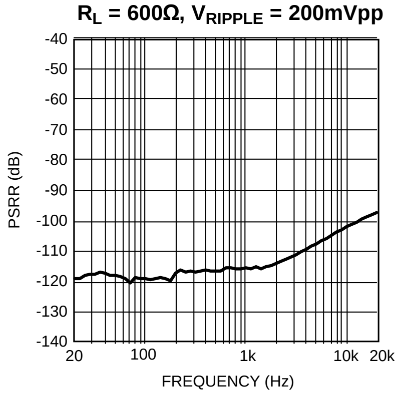
PSRR+ vs Frequency
V_{CC} = 15V, V_{EE} = –15V, R_L = 600Ω, V_{RIPPLE} = 200mVpp



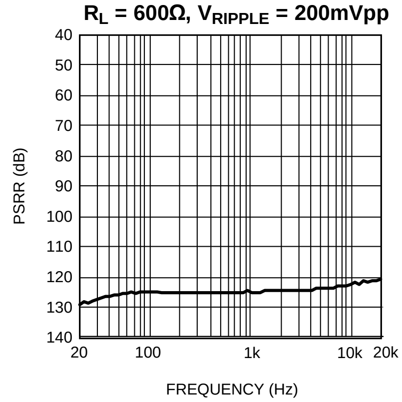
PSRR- vs Frequency
V_{CC} = 15V, V_{EE} = –15V, R_L = 600Ω, V_{RIPPLE} = 200mVpp



PSRR+ vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 600Ω, V_{RIPPLE} = 200mVpp

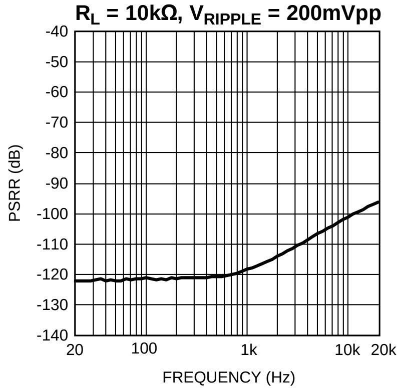


PSRR- vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 600Ω, V_{RIPPLE} = 200mVpp

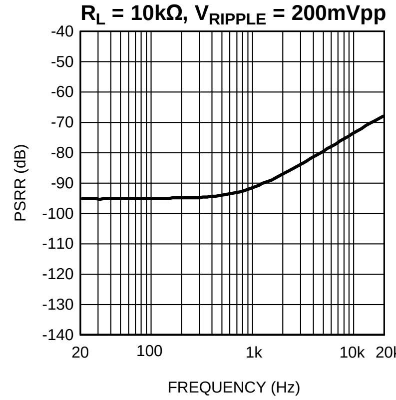


Typical Performance Characteristics (continued)

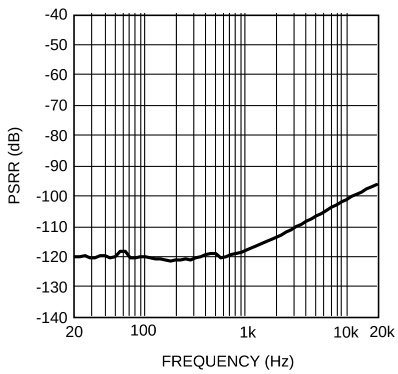
PSRR+ vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 10kΩ, V_{RIPPLE} = 200mVpp



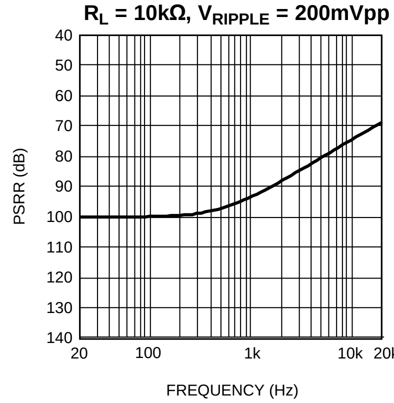
PSRR- vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 10kΩ, V_{RIPPLE} = 200mVpp



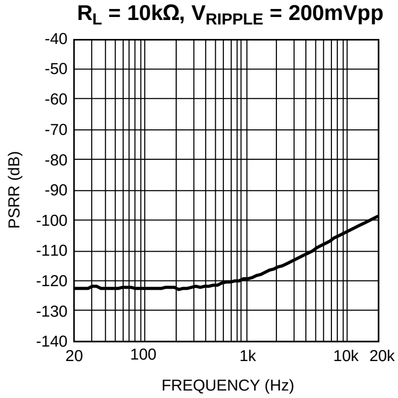
PSRR+ vs Frequency V_{CC} = 12V, V_{EE} = –12V, R_L = 10kΩ, V_{RIPPLE} = 200mVpp



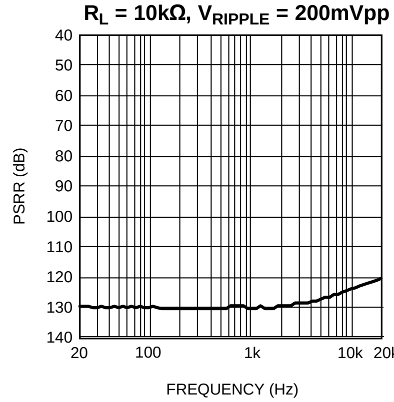
PSRR- vs Frequency V_{CC} = 12V, V_{EE} = –12V, R_L = 10kΩ, V_{RIPPLE} = 200mVpp



PSRR+ vs Frequency V_{CC} = 15V, V_{EE} = –15V, R_L = 10kΩ, V_{RIPPLE} = 200mVpp



PSRR- vs Frequency V_{CC} = 15V, V_{EE} = –15V, R_L = 10kΩ, V_{RIPPLE} = 200mVpp



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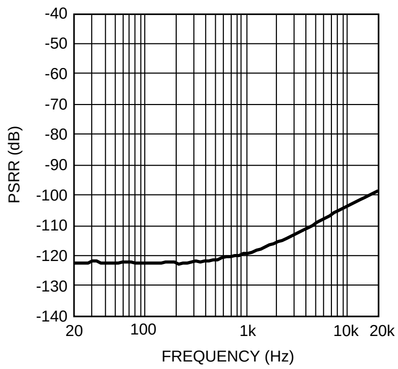
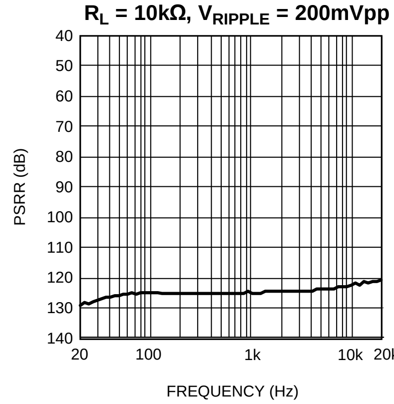
Typical Performance Characteristics (continued)

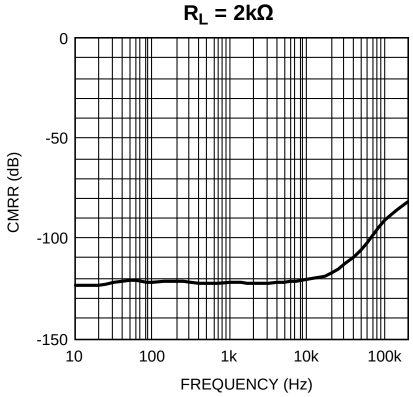
PSRR+ vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 10kΩ, V_{RIPPLE} = 200mVpp



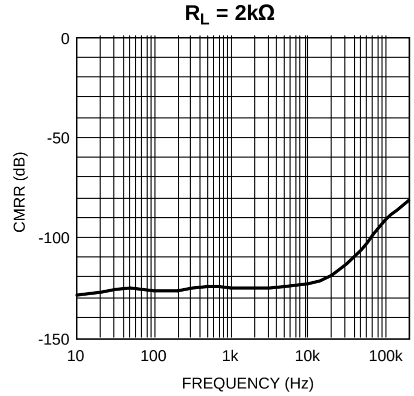
PSRR- vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 10kΩ, V_{RIPPLE} = 200mVpp



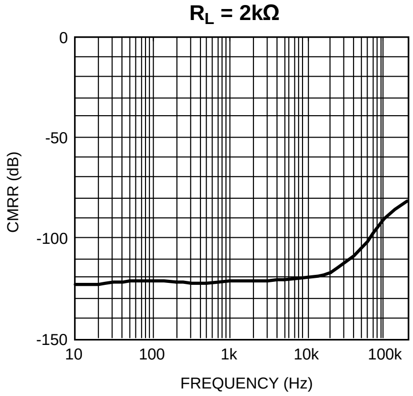
CMRR vs Frequency
V_{CC} = 15V, V_{EE} = –15V, R_L = 2kΩ



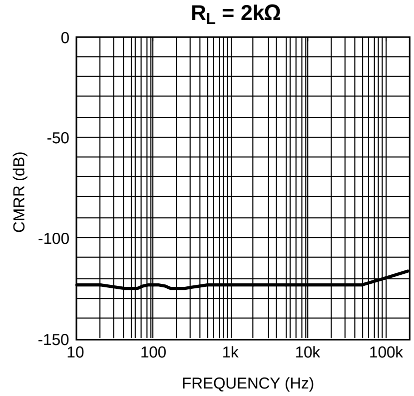
CMRR vs Frequency
V_{CC} = 12V, V_{EE} = –12V, R_L = 2kΩ



CMRR vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 2kΩ



CMRR vs Frequency
V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 2kΩ



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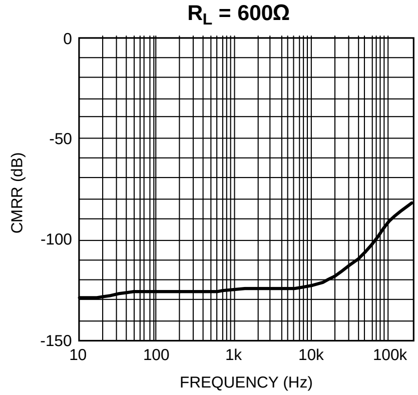
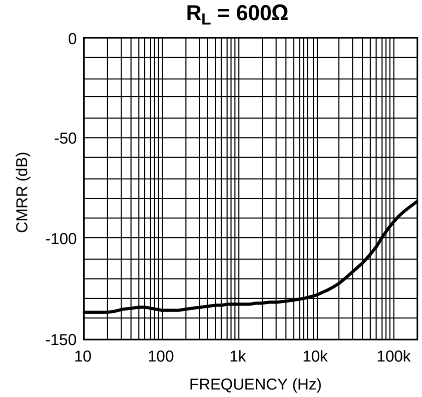
Typical Performance Characteristics (continued)

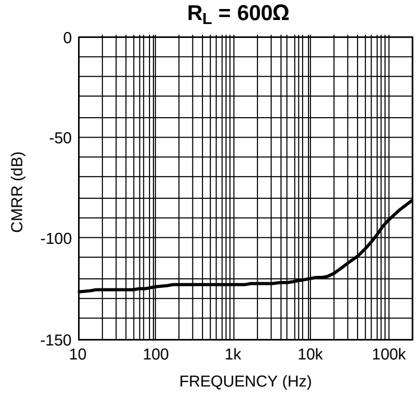
CMRR vs Frequency V_{CC} = 15V, V_{EE} = –15V, R_L = 600Ω



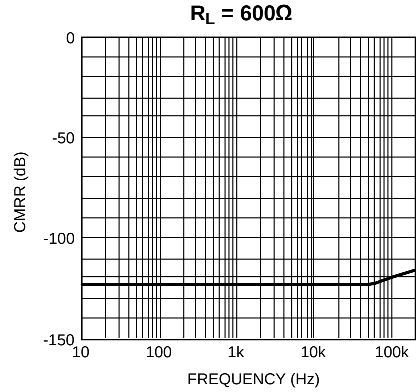
CMRR vs Frequency V_{CC} = 12V, V_{EE} = –12V, R_L = 600Ω



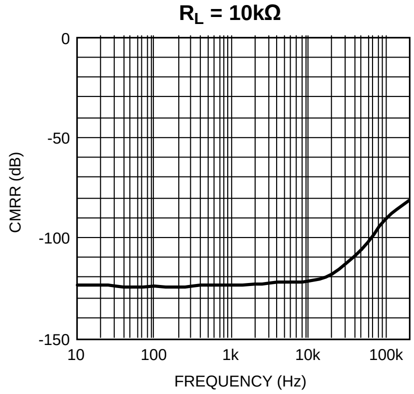
CMRR vs Frequency V_{CC} = 17V, V_{EE} = –17V, R_L = 600Ω



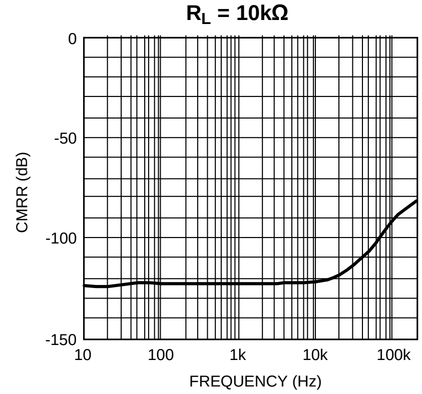
CMRR vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 600Ω



CMRR vs Frequency V_{CC} = 15V, V_{EE} = –15V, R_L = 10kΩ



CMRR vs Frequency V_{CC} = 12V, V_{EE} = –12V, R_L = 10kΩ



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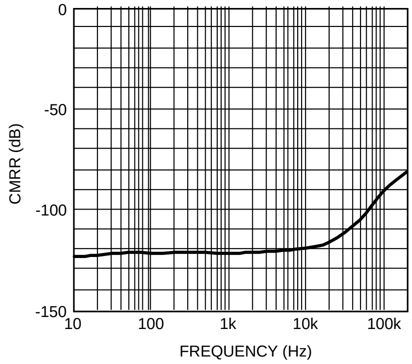
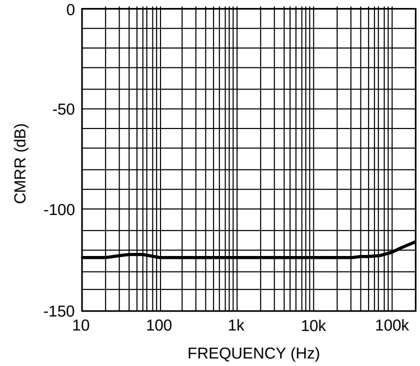
Typical Performance Characteristics (continued)

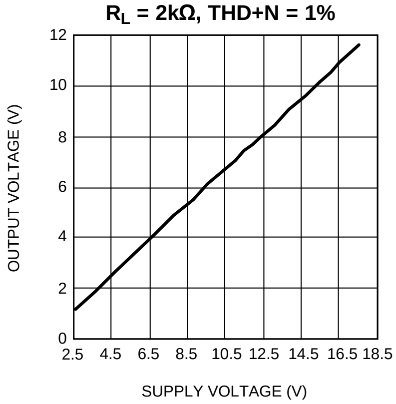
CMRR vs Frequency
V_{CC} = 17V, V_{EE} = –17V, R_L = 10kΩ



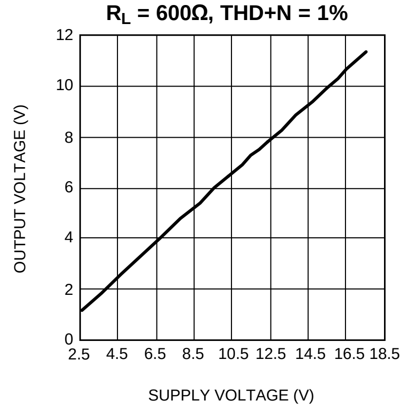
CMRR vs Frequency
V_{CC} = 2.5V, V_{EE} = –2.5V, R_L = 10kΩ



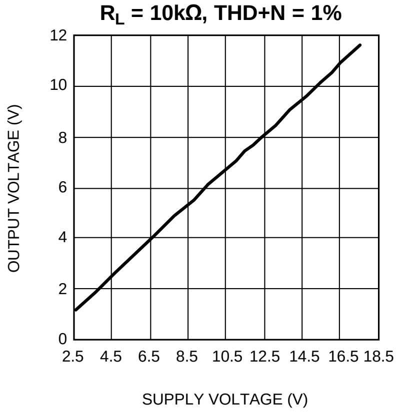
Output Voltage vs Supply Voltage
R_L = 2kΩ, THD+N = 1%



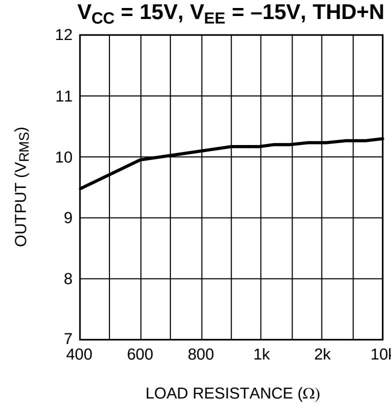
Output Voltage vs Supply Voltage
R_L = 600Ω, THD+N = 1%



Output Voltage vs Supply Voltage
R_L = 10kΩ, THD+N = 1%

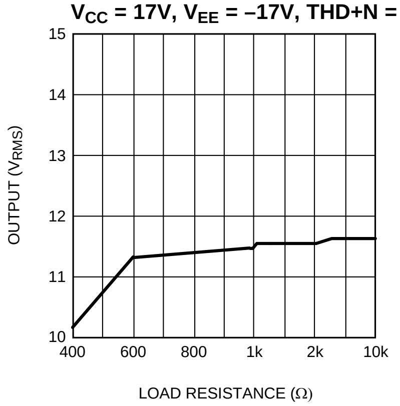


Output Voltage vs Load Resistance
V_{CC} = 15V, V_{EE} = –15V, THD+N = 1%

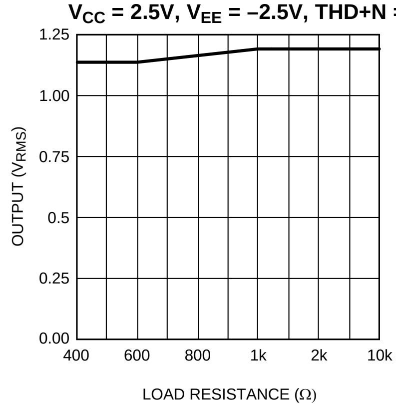


Typical Performance Characteristics (continued)

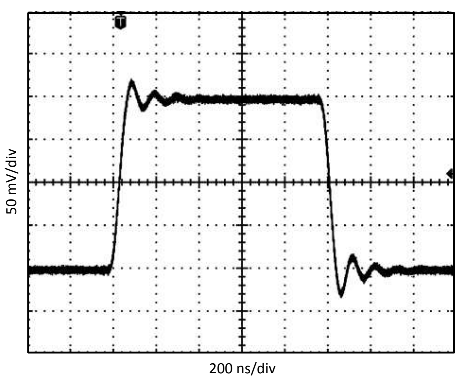
Output Voltage vs Load Resistance
V_{CC} = 17V, V_{EE} = –17V, THD+N = 1%



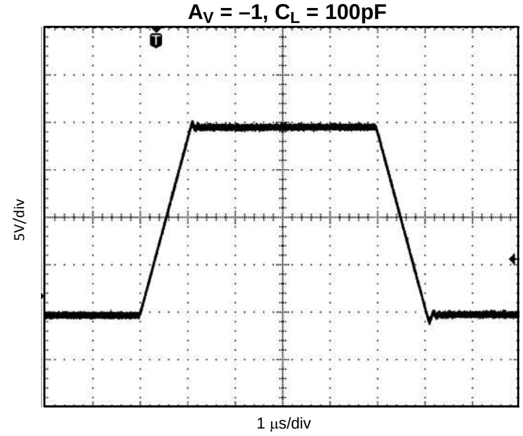
Output Voltage vs Load Resistance
V_{CC} = 2.5V, V_{EE} = –2.5V, THD+N = 1%



Small-Signal Transient Response
A_V = –1, C_L = 100pF



Large-Signal Transient Response
A_V = –1, C_L = 100pF



Application Hints

The LME49710 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straight forward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

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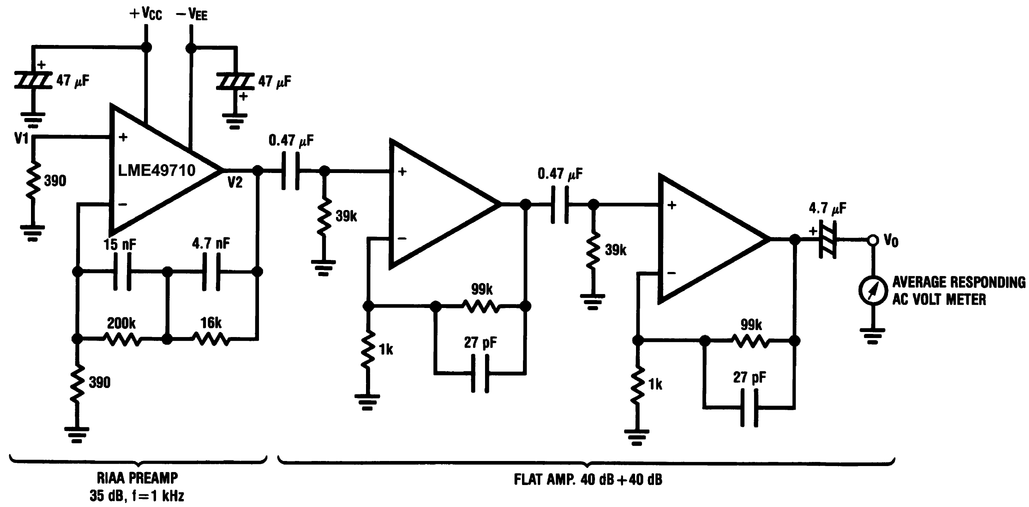
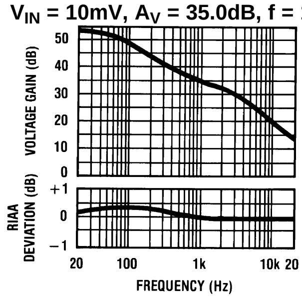
Noise Measurement Circuit



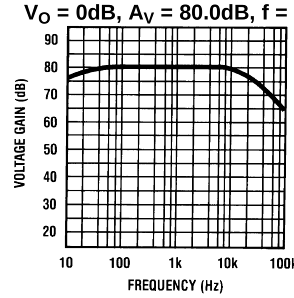
Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.

Figure 4. Total Gain: 115 dB at f = 1 kHz
Input Referred Noise Voltage: $e_n = V_O/560{,}000$ (V)

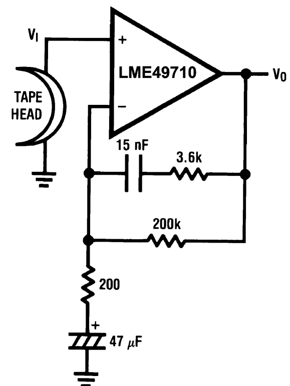
RIAA Preamp Voltage Gain
RIAA Deviation
vs
Frequency
V_{IN} = 10mV, A_V = 35.0dB, f = 1kHz



Flat Amp Voltage Gain
vs
Frequency
V_O = 0dB, A_V = 80.0dB, f = 1kHz



Typical Applications



A_V = 34.5
F = 1 kHz
E_n = 0.38 μV
A Weighted

Figure 5. NAB Preamp

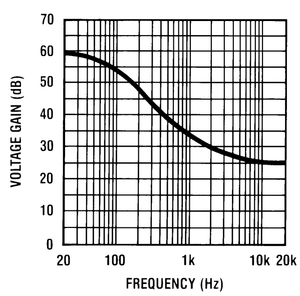


Figure 6. NAB Preamp Voltage Gain vs Frequency
V_{IN} = 10mV, 34.5dB, f = 1kHz

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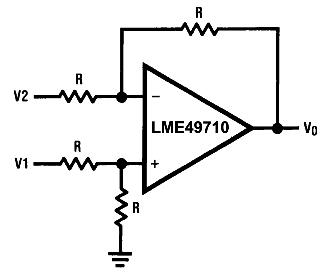
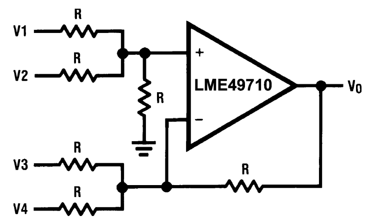


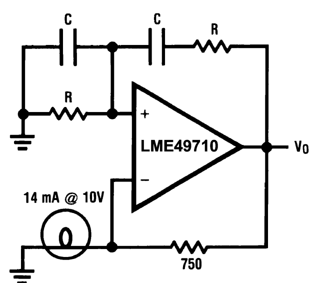
V_O = V1–V2

Figure 7. Balanced to Single Ended Converter



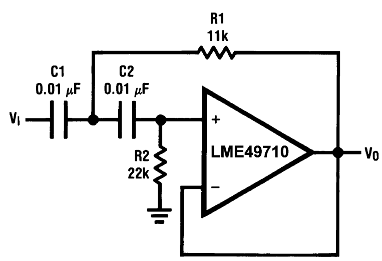
V_O = V1 + V2 − V3 − V4

Figure 8. Adder/Subtracter



$$f_o = \frac{1}{2\pi RC}$$

Figure 9. Sine Wave Oscillator



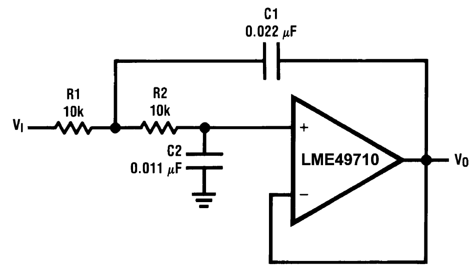
if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_0 C}$$

R2 = 2•R1

Illustration is f_0 = 1 kHz

Figure 10. Second Order High Pass Filter (Butterworth)



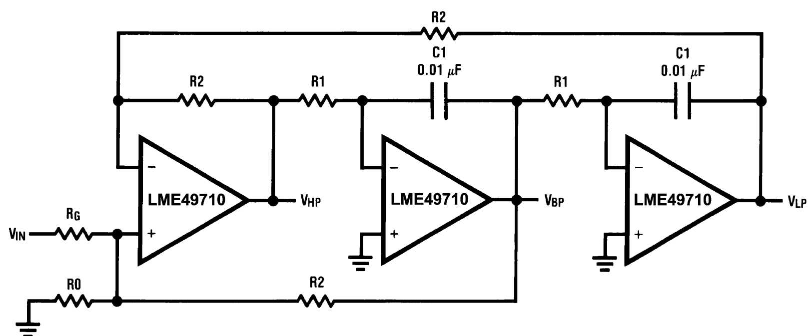
if R1 = R2 = R

$$C1 = \frac{\sqrt{2}}{\omega_0 R}$$

$$C2 = \frac{C1}{2}$$

Illustration is f_0 = 1 kHz

Figure 11. Second Order Low Pass Filter (Butterworth)



$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

Figure 12. State Variable Filter

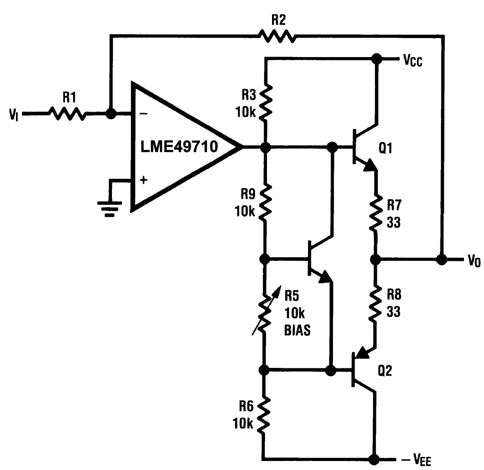


Figure 13. Line Driver

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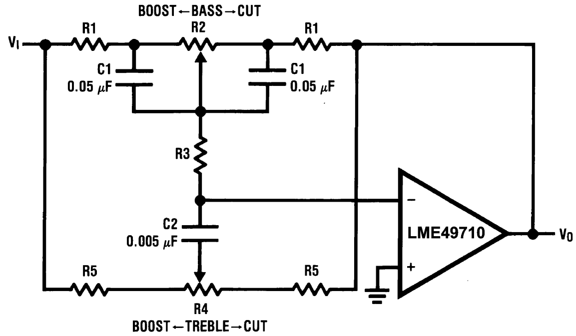


$$f_L = \frac{1}{2\pi R2C1}, f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2}, f_{HB} = \frac{1}{2\pi (R1 + R5 + 2R3)C2}$$

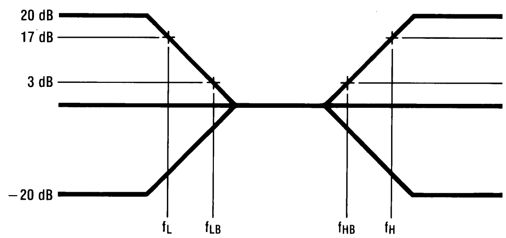
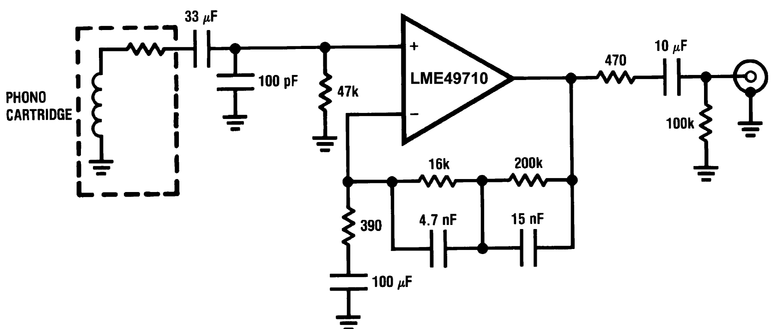
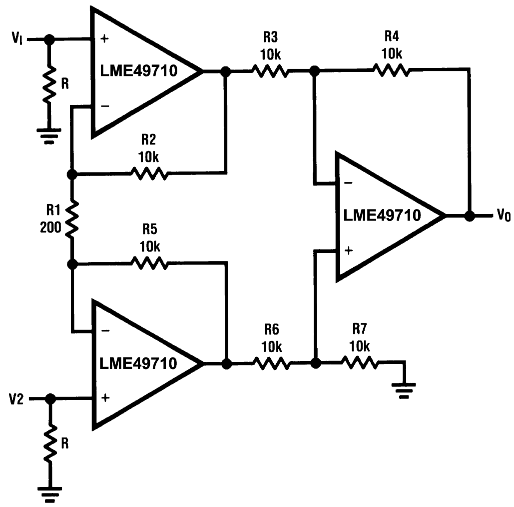


Figure 14. Tone Control



A_v = 35 dB
E_n = 0.33 μV
S/N = 90 dB
f = 1 kHz
A Weighted
A Weighted, V_{IN} = 10 mV
@f = 1 kHz

Figure 15. RIAA Preamp



If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:

V0 = 101(V2 − V1)

Figure 16. Balanced Input Mic Amp

Application Information

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49710 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49710's low residual distortion is an input referred internal error. As shown in Figure 17, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 17.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

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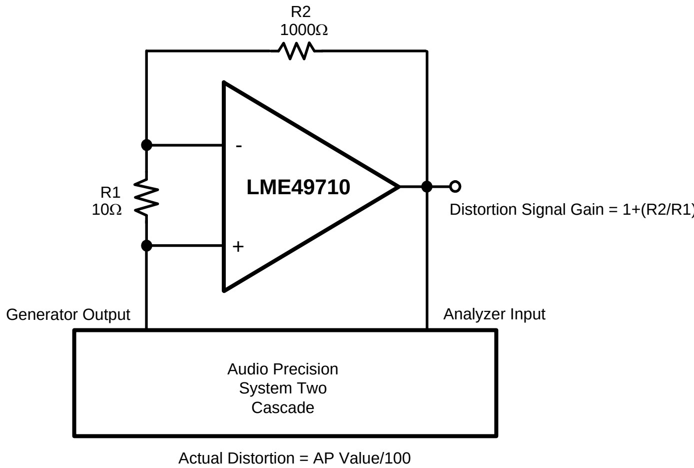

Figure 17. THD+N and IMD Distortion Test Circuit

Revision History

Rev	Date	Description
1.0	11/16/07	Initial release.
1.1	12/12/06	Added the Typical Performance curves.
1.2	01/15/07	Added more curves and input some text edits.
1.3	03/09/07	Fixed graphics 20210489 and 90.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LME49710HA/NOPB	ACTIVE	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-40 to 85		Samples
LME49710MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L49710 MA	Samples
LME49710MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L49710 MA	Samples
LME49710NA/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LME 49710NA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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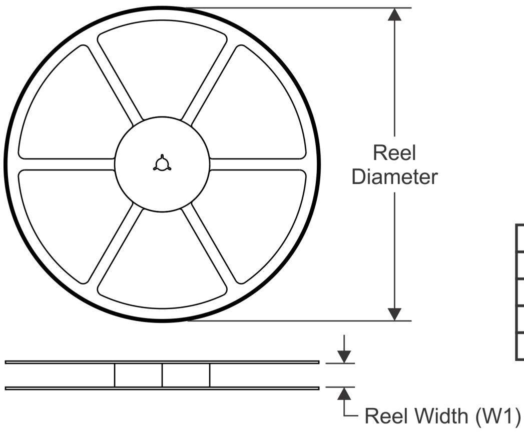
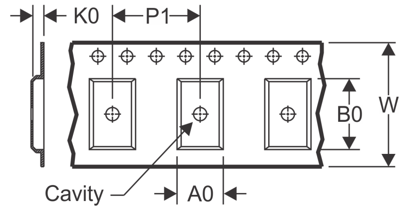
TAPE AND REEL INFORMATION

REEL DIMENSIONS

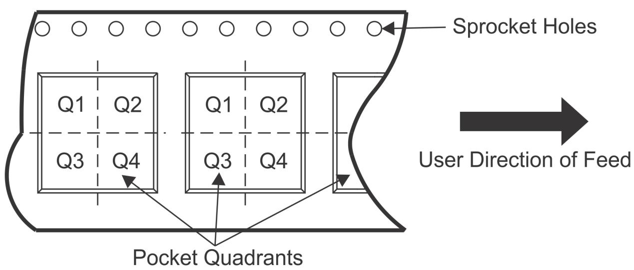


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

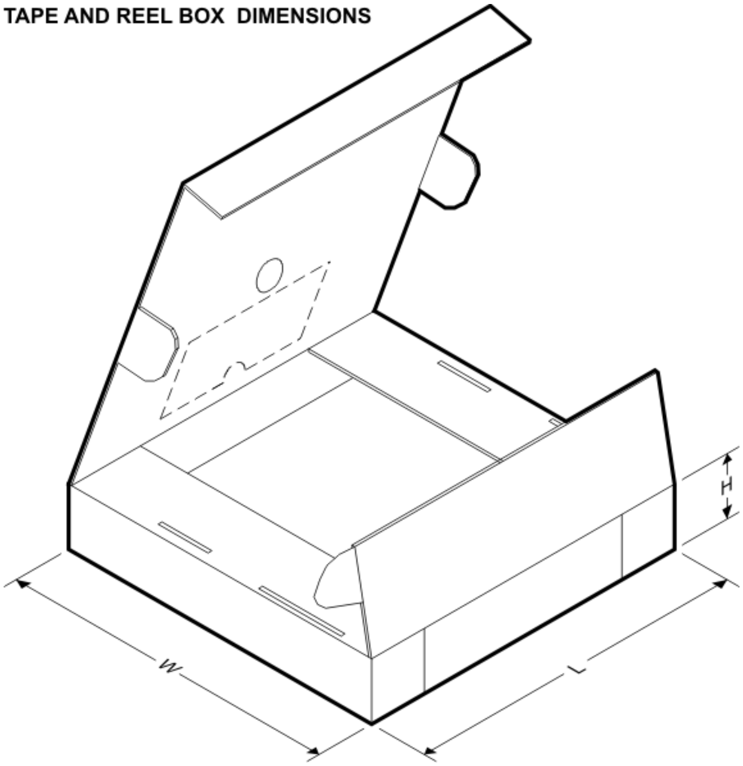
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49710MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

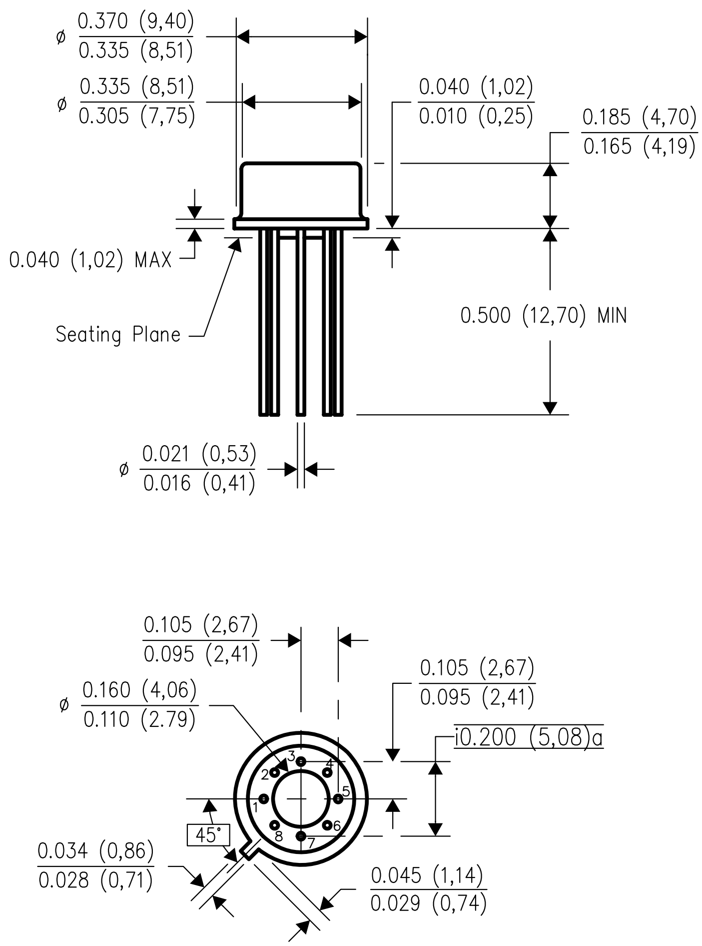
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49710MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

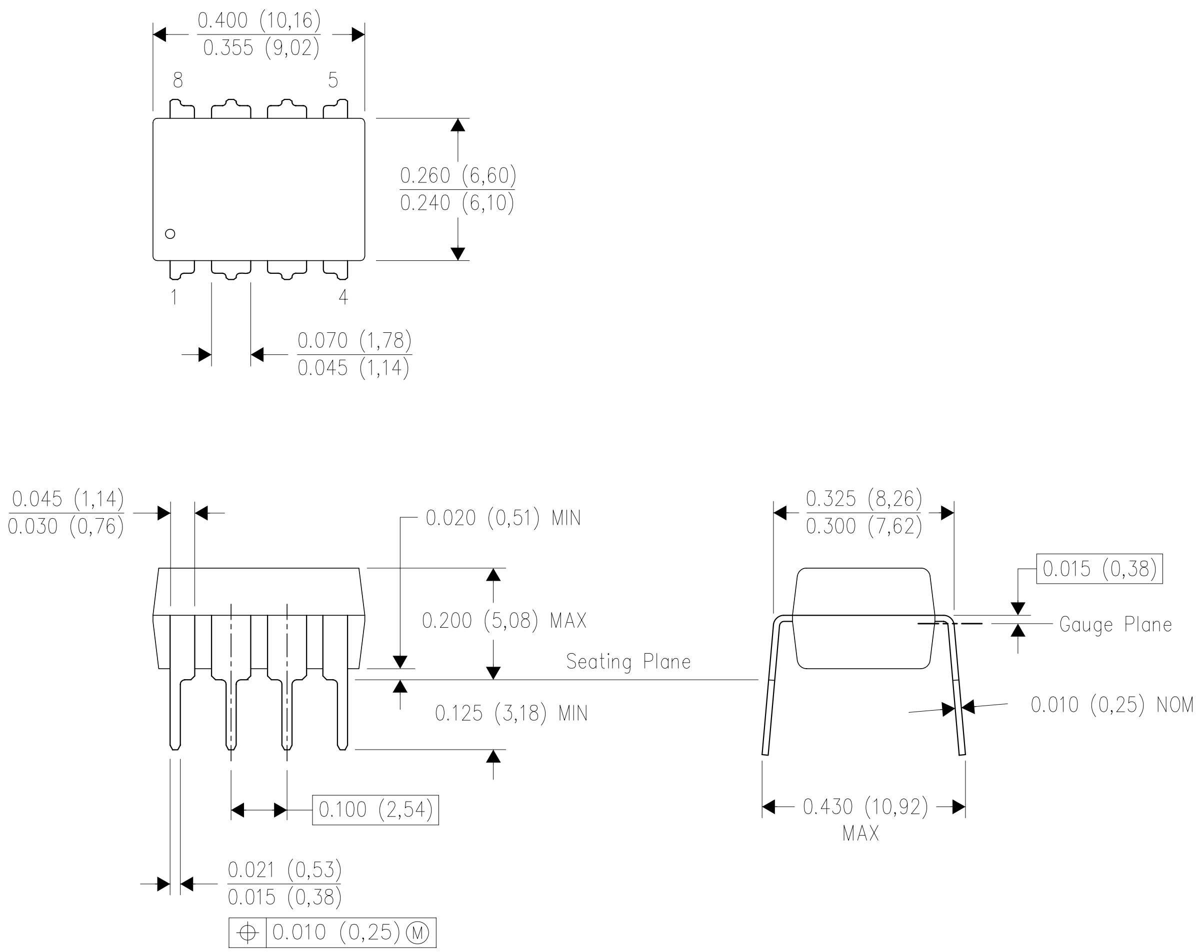
LMC (O-MBCY-W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
- D. Pin numbers shown for reference only. Numbers may not be marked on package.
- E. Falls within JEDEC MO-002/TO-99.

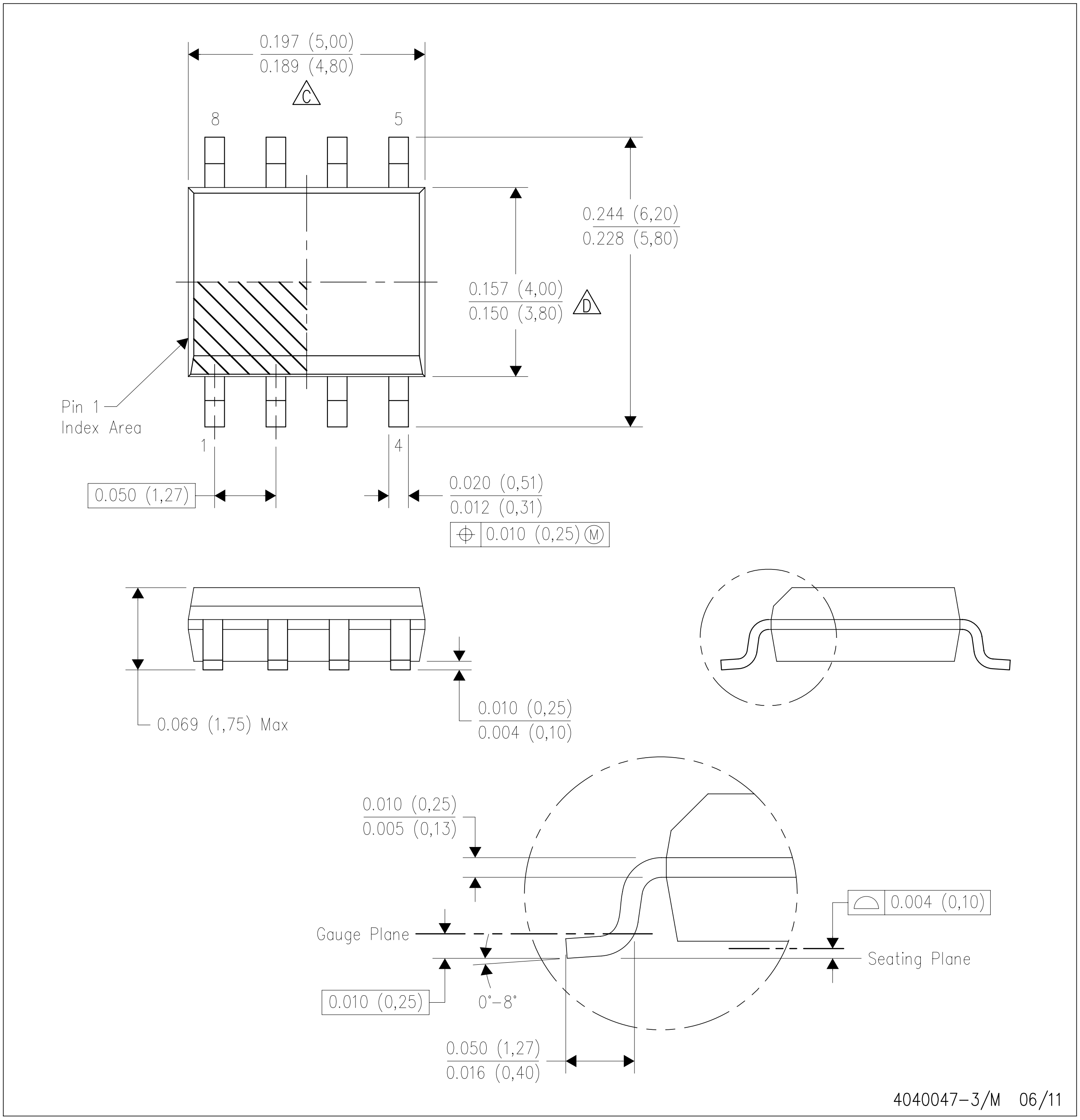
P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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